



(use as many sheets as necessary)

Sheet	1	of	1
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**Complete if Known**

Application Number	10/656,628
Filing Date	September 5, 2003
First Named Inventor	Yoshihide SENZAKI
Art Unit	2812-1762
Examiner Name	Not yet assigned
Attorney Docket Number	A-71730/MSS (463035-878)

## U.S. PATENT DOCUMENTS

## FOREIGN PATENT DOCUMENTS

Examiner Signature		Date Considered	9/26/05
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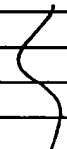
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<b>Substitute for form 1449A/PTO (Modified)</b>  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)			<b>Complete if Known</b>		
			Application Number	10/656,628	
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			First Named Inventor	Yoshihide SENZAKI	
			Art Unit	2842 1762	
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Sheet	1	of	3	Attorney Docket Number	A-71730/MSS


U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No.	Document Number Number-Kind Code <sup>2</sup> (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	A1	4,239,811	12-16-1980	Kemlage	
	A2	4,720,395	01-19-1988	Foster	
	A3	5,032,545	07-1991	Doan et al.	
	A4	5,478,765	12-26-1995	Kwong et al.	
	A5	5,576,059	11-19-1996	Beinglass et al.	
	A6	5,578,848	12-26-1995	Kwong et al.	
	A7	5,744,196	04-28-1998	Laxman et al.	
	A8	5,874,368	02-23-1999	Laxman et al.	
	A9	5,932,286	08-03-1999	Beinglass et al.	
	A10	6,114,662	09-2000	Guidotti et al.	
	A11	6,150,286	11-21-2000	Sun et al.	
	A12	6,153,261	11-28-2000	Xia et al.	
	A13	2003-0104707 A1	06-05-2003	Senzaki	
	A14	2001-0003381 A1	06-14-2001	Orlowski et al.	

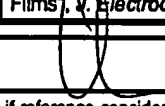
FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No.	Foreign Patent Document Country Code* Number* Kind Code* (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T
	B1	EP 0 260 473 A1	03-23-1988	IBM		
	B2	EP 1 047 117 A2	10-25-2000	Oki Electric Ind. Co. Ltd.		

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NON PATENT LITERATURE DOCUMENTS				
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume/issue number(s), publisher, city and/or country where published.		T*
	C1	Author Unknown, "Wafer Processing News: Nitride Gate Dielectric, Poly/W Electrode Enable 100nm CMOS", 2000, Cahners Semiconductor International, at <a href="http://www.semiconductor.net/semiconductor/issues/issues/2000/20001/six001wp.asp">http://www.semiconductor.net/semiconductor/issues/issues/2000/20001/six001wp.asp</a> , p. 1.		
	C2	ERIGUCHI, K., et al., "Role of Base Layer in CVD Si <sub>3</sub> N <sub>4</sub> Stack Gate Dielectrics on the Process Controllability and Reliability in Direct Tunneling Regime", <i>IEEE</i> , 1999, pp. 323-326.		
	C3	HENDA, R., et al., "Characterization of Chemically Vapor Deposited Silicon Nitride Films from Disilane and Ammonia", <i>Jpn. J. Appl. Phys.</i> , April 1, 1995, Vol. 34, Part 2, No. 4A: L437-L439.		
	C4	HENDA, R., et al., "Experimental and chemical kinetic study of silicon nitride via LPCVD at low temperature from disilane and ammonia", <i>Journal De Physique IV</i> , 1993, 3: 395-402.		
	C5	HENDA, R., et al., "Kinetics of the Low Pressure Chemical Vapor Deposition of Stoichiometric Silicon Nitride at Low Temperature from Disilane and Ammonia", <i>Journal of Chemical Vapor Deposition</i> , January 1993, 1: 300-314.		
	C6	KIM, B.Y., et al., "Ultra Thin (<3 nm) High Quality Nitride/Oxide Stack Gate Dielectrics Fabricated in In-Situ Rapid Thermal Processing", <i>IEEE</i> , 1997, pp. 463-466.		
	C7	LASER, A., et al., "Hot Wall Isothermal RTO for gate Oxide Growth and Nitridation", <i>Mat. Res. Soc. Meeting</i> , April 2000, Abstract C7.7.		
	C8	LAXMAN, R.K., et al., "A low-temperature solution for silicon nitride deposition", <i>Solid State Technology</i> , April 2000, 79-87.		
	C9	LEE, E., "Investigation of microstructure and grain growth of polycrystalline silicon deposited using silane and disilane", <i>Thin Solid Films</i> , 1993, 226:123-128.		
	C10	LEVY, S., et al., "Solutions for the 100nm Node with Ultrathin Silicon Nitride Gates", <i>Solid State Technology</i> , April 2001, pp. 75-80.		
	C11	MIZUNO, Y., et al., "Analysis of reaction gases flow in CVD processes", <i>Materials Science and Engineering</i> , 1995, B35: 156-159.		
	C12	OLIVARES, J., et al., "Effect of Deposition Parameters on the Characteristics of Low-Pressure Chemical Vapor Deposited SiGe Films Grown from Si <sub>2</sub> H <sub>6</sub> and GeH <sub>4</sub> ", <i>Journal of The Electrochemical Society</i> , 2001, 148(10):C685-C-689.		
	C13	ONAI, T., et al., "0.1 μm CMOS Technology for High-Speed Logic and System LSIs with SiO <sub>2</sub> /Si/poly-Si/W Gate System", <i>IEEE</i> , 1999, pp. 937-938.		
	C14	SENZAKI, Y., et al., "Single-wafer furnace RTCVD for silicon oxide, nitride, and oxynitride thin films", <i>9<sup>th</sup> Int. Conference on Advanced Thermal Processing of Semiconductors</i> , RTP 2001 (Cat. No. 02EX513), Anchorage, Alaska, 25-29 Sept. 2001, pages 197-200.		
	C15	SONG, S.C., et al., "Ultra Thin (<20 Å) CVD Si <sub>3</sub> N <sub>4</sub> Gate Dielectric for Deep-Sub-Micron CMOS Devices", <i>IEEE</i> , 1998, pp. 373-376.		
	C16	SONG, S.C., et al., "Ultra Thin High Quality Stack Nitride/Oxide Gate Dielectrics Prepared by In-Situ Rapid thermal N <sub>2</sub> O Oxidation of NH <sub>3</sub> -nitrided Si", republished in <i>Elsevier Science B.V., Microelectronic Engineering</i> , 1999, 48: 55-58.		
	C17	SONG, S.C., et al., "Ultra Thin High Quality Stack Nitride/Oxide Gate Dielectrics Prepared by In-Situ Rapid thermal N <sub>2</sub> O Oxidation of NH <sub>3</sub> -nitrided Si", <i>Symposium on VLSI Technology Digest of Technical Papers</i> , 1999, pp. 137-138.		
	C18	TANAKA, M., et al., "Film Properties of Low-k Silicon Nitride Films Formed by Hexachlorodisilane and Ammonia", <i>Journal of The Electrochemical Society</i> , 2000, 147(6): 2284-2289.		
	C19	TAYLOR, R.C., et al., "Hexachlorodisilane as a Precursor in the LPCVD of Silicon Dioxide and Silicon Oxynitride Films", <i>J. Electrochem. Soc.</i> , August 1989, 136(8): 2382-2385.		

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**10/656.628**

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First Named Inventor

Yoshihide SENZAKI

**Art Unit**

2812

Examiner Name \_\_\_\_\_

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## NON PATENT LITERATURE DOCUMENTS

[illegible]

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